0975024 to *Bridge-Butler, et al.* Reconsideration of pending 1-9 claims and withdrawal of the rejections are respectfully requested in view of the above amendments and the remarks which follow.

A. Specification Objection Addressed by Submittal of Substitute Specification.

The minor specification objections and awkward grammatical phrasing resulting from translation of the specification have been corrected in a substitute specification enclosed herewith. Also enclosed is a marked-up copy of the specification showing the amendments made. No new matter has been introduced. Please note, however, that to avoid confusion, the enclosed substitute specification does not include drawings (which remain the same as originally filed) or claims (some of which have been amended herein). Confirmation of entry of the enclosed substitute specification is respectfully requested.

B. 35 U.S.C. § 112 Rejections of Claims 1, 5 and 6 Addressed.

The rejection of claim 5 under 35 U.S.C. § 112, 1st paragraph, is respectfully traversed. The subject matter of claim 5 is believed sufficiently described to comply with 35 U.S.C. § 112, 1st paragraph, at page 5, line 27 though page 6, line 2 (as amended) with the following language:

> . . . . p type columns 13 are optimally doped to balance the charge on n type zone 10. When this condition is reached, the electric field upon the entire volume of the drain region 10 is constant and it is also equal to the critical electric field of the silicon.

Doping, and the associated charges resulting from doping with n type and p type materials in a semiconductor layer are well established in the semiconductor arts. Therefore the description spanning pages 5 and 6 referenced above is believed to be enabling to those of ordinary skill in the semiconductor arts. Claim 5 is thus believed to be fully enabled.

Claims 1 and 6 stand rejected under 35 U.S.C. § 112, 2nd paragraph. Claims 1 and 6 have been amended to address the detailed rejection points raised by the Examiner and the § 112, 2nd paragraph rejection is thereby addressed. No new matter is included in the amendments.

C. <u>Anticipation Rejection of Claims 1-6, 8 and 9 over *Werner*, Obviousness Rejection of Claims 1 and 7 over *Werner*, and Anticipation Rejection of Claims 1-9 over *Bridge-Butler* Addressed</u>.

Claims 1-6, 8 and 9 stand rejected under 35 U.S.C. §102(e) as anticipated by *Werner*, claims 1 and 7 stand rejected under U.S.C. §103 as obvious over *Werner,* and claims 1-9 stand rejected under 35 U.S.C. §102(e) as anticipated by *Bridge-Butler.* These substantive rejections of claims 1-9, as now amended, are respectfully traversed.

More particularly, claim 1 has been amended to recite a limitation that the doped regions are separated from each other <u>and from the substrate</u>. Support for this limitation is shown in FIGS. 2 and 3 and corresponding description in the specification. No new matter has been added.

Werner discloses a semiconductor component, such as a Schottky diode with a low leakage current, which has a metal-semiconductor junction between a first metal electrode and the semiconductor. The semiconductor, which is of the first conductivity type, has a defined drift path and a plurality of supplementary zones of a second conductivity type extending from the semiconductor surface into the drift path. A number of foreign atoms in the supplementary zones is substantially equal to a number of foreign atoms in intermediate zones surrounding the supplementary zones and the number of foreign atoms does not exceed a number corresponding to a breakdown charge of the semiconductor.

Bridge-Butler discloses a semiconductor device including a semiconductor substrate region 32, through which a current flows in the ON-state of the device and which is depleted in the OFF-state. The semiconductor substrate region 32 includes a plurality of vertical alignments of n-type buried regions 32b and a plurality of vertical alignments of p-type buried regions 32c. The vertical aligned n-type buried regions 32b and the vertically aligned p-type buried regions 32c are alternately arranged horizontally. The n-type buried regions 32b and n-type buried regions 32c are formed by diffusing respective impurities into highly resistive n-type layers 32a laminated one by one epitaxially.

In contrast, amended claim 1 of the pending patent application

comprises a substrate region 9 of the first conductivity type formed in a semiconductor material layer of the same conductivity type, a metal layer 12 and at least two doped regions 13 of the second conductivity type formed in said semiconductor material layer. Each one of the doped regions is placed under the metal layer and is separated from the other doped region by portion of the semiconductor layer.

The semiconductor material layer comprises a heavily doped substrate 9 and a layer 10 grown epitaxially over the substrate 9. Each doped region 13 is placed inside the layer 10 in a way wherein the upper part of the region 13 is in contact with the top surface of the layer 10 while a portion of layer 10 is placed between the bottom of the region 13 and the substrate 9.

This feature is not present in cited prior art and allows the electric field to be not very high at the interface between the layers 9 and 10 in order to limit the breakdown of the device.

Because amended claim 1 is patentably distinguishable over both *Werner* and *Bridge-Butler*, it is allowable over these references. Claims 2-9 are also believed to be allowable as being dependent from an allowable base claim. Accordingly, withdrawal of the § 102 and § 103 rejections of claims 1-9 is respectfully requested.

D. Conclusion.

Although no fee is believed due for this filing, any fee deficiency associated with this transmittal may be charged to Deposit Acct. No. 50-1123.

Respectfully submitted,

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MARKED UP COPY OF AMENDED CLAIMS

1. (Amended) A Schottky barrier diode comprising:

a substrate region of a first conductivity type formed [in] underneath a semiconductor material layer of the same conductivity type;

a metal layer; and

at least two doped regions of a second conductive type formed in said semiconductor material layer, each one of said doped regions being disposed under said metal layer and being separated from the other doped region and said substrate region by portions of said semiconductor layer.

6. (Amended) The Schottky barrier diode according to claim 1, in which said [body] doped regions further comprise heavily doped body regions having the same conductivity type of said doped regions.

MARKED UP COPY OF SUBSTITUTE SPECIFICATION

SILICON IMPROVED SCHOTTKY BARRIER DIODE

BACKGROUND OF THE INVENTION

The present invention relates to a silicon improved Schottky barrier diode, particularly to a Schottky barrier diode of high - voltage with a Multi Drain (MD) technology.

Schottky barrier diodes (generally indicated as SBD) are used as voltage rectifiers in many power switching applications. In fact whenever a current is switched to an inductive load, such as an electric motor, high - voltage transients on the conductive lines are induced.

Usually to suppress these transients, that is to rectify a waveform, a PN junction diode [PN] is used, and said PN diode [PN] is placed across each switching means, for example a power transistor, to clamp the voltage excursions.

PN junction diodes can be used for this application, but they store minority carriers when forward biased, and the extraction of these carriers generates a reverse current having a large transient during switching.

In switching applications, the PN diode is turned on and off by fast pulses, and the reverse recovery finite time limits the rate of pulses that can be applied, thus limiting the diode switching speed.

To overcome these drawbacks a metal - semiconductor rectifying junction, called MSJ, is used.

In this type of device, [due to their internal physic phenomenon,] the forward current consists of majority carriers injected from the semiconductor into the metal.

Consequently, MSJs do not store minority carriers when forward

biased, and the reverse current transient is negligible. This means that the MSJ can be turned off faster than a PN diode, and therefore they dissipate a negligible power during switching.

However the on - resistance of the MSJ increases sharply with the growth of the voltage, and this occurrence limits their use to a voltage range of about 150 V - 200 V.

In ultra fast switching applications, over 200 V, mainly a bipolar diode is used. This diode is responsible for an important part of the dissipated power due mainly to the drain epitaxial layer resistance, and the dissipated power depends, also, on the doping concentration of the epitaxial layer itself.

In fact the power dissipation occurs in this type of diode during the conduction phase. If the working frequency increases, the power dissipation occurs more and more during the off - commutation. Power dissipation occurs not only in the diode, but also in [the parasite] a parasitic MOS[,] transistor due to the diode charge recovery phenomenon.

In view of the state of the art described, it is an object of the present invention to provide a device able to suppress voltage transients, to work at high - voltage and to limit [the] power dissipation.

It is another object of the present invention to propose an alternative device [respect] to [the] bipolar diodes in ultra fast switching applications.

SUMMARY OF THE INVENTION

According to the present invention, such objects are achieved by a Schottky barrier diode comprising a substrate region of a first conductivity type formed in a semiconductor material layer of the same conductivity type and a metal layer, characterized in that at least a doped region of a second conductive type is formed in said semiconductor material layer,

each one of said doped regions being disposed under said metal layer and being separated from other doped regions by portions of said semiconductor material layer. [Thanks] According to the present invention it is possible to make a Schottky barrier diode having an higher voltage breakdown. Moreover, [thanks] according to the present invention it is possible to make a Schottky barrier diode having a lower on - resistance with respect to the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and the advantages of the present invention will be made evident by the following detailed description of an embodiment thereof, which is illustrated as [not] a non-limiting example in the annexed drawings, wherein:

Figure 1 shows a schematic cross sectional view of a Schottky barrier diode according to the prior art;

Figure 1A shows the relationship between the breakdown voltage and the on - resistance according to the prior art;

Figure 2 shows a first embodiment of a Multi Drain Schottky barrier diode according to the present invention;

Figure 3 shows a second embodiment of a Multi Drain Schottky barrier diode according to the present invention;

Figure 4A shows another schematic cross sectional view of the Schottky barrier diode according to the prior art;

Figure 4 shows a top plan view of the first embodiment of Figure 2;

Figure 5 shows a cross sectional view of the first embodiment of Figure 2 along the line V - V.

DETAILED DESCRIPTION

In Figure 1 a schematic cross sectional view of a Schottky barrier diode according to the prior art is shown. This device, indicated as 1, employs [a] an n - type epitaxial layer 2 on an n^+ - type substrate 3, to reduce the diode series resistance.

The resistivity values and the thickness of a device adapted to sustain a voltage in a range between 100 V and 500 V[,] must be in a range of resistivity between 5 Ohm * cm and 20 Ohm * cm and in a range of thickness between 15 μm and 50 μm.

[The diode] Diode 1 is fabricated by depositing a metal layer 4 of suitable size onto the n - type epitaxial layer 2, and by producing a metal - semiconductor contact 5, called an ohmic contact. Said ohmic contact has a resistance negligibly small compared with the resistance of the n^+ - type substrate 3 to which the ohmic contact itself is applied.

The metal layer 4 represents a first electrode 6, called the anode, and the ohmic contact 5 represents a second electrode 7, called the cathode.

[The device] Device 1 [shows] has a large leakage reverse [large] current and it has a low breakdown voltage because of the concentration of the electric field near the periphery of the device.

Moreover, the on - resistance of [the] diode 1 increases sharply with the growth of the voltage, and this occurrence limits [their] its use to a range of voltage between 150 V - 200 V.

In fact the law that links the voltage breakdown with the epitaxial layer resistivity is: $BV \propto \rho^{3/4}$, where BV is the breakdown voltage and ρ is the epitaxial layer resistivity.

Such a formula is shown in the graph of Figure 1A, wherein there is an abscissa axis illustrating the breakdown voltage expressed in V and an ordinate axis illustrating the on - resistance of the active area expressed in

mOhm * cm^2.

To overcome these problems [the Applicant has found that to obtain] a Schottky barrier diode with a low on - resistance and a high breakdown voltage [it is necessary to produce devices] with drain layers comprising a Multi Drain structures, according to the present invention, as shown in Figure 2.

In this way [the Applicant has realized] a device having [an] a higher voltage capability for a given epitaxy doping level, [an] a higher voltage breakdown and a lower on - resistance with respect to [the] known devices is realized.

In Figure 2 a cross sectional view of a first embodiment of a Multi Drain Schottky barrier diode according to the present invention is shown.

As shown in [such] Figure 2, the new device 8 comprises a heavily dopedsubstrate 9 [heavily doped,] onto which a semiconductor layer 10 is formed, for example by [an] epitaxial growth. In a specific embodiment, either [the] substrate 9 and/or [the] semiconductor layer 10 are of n type conductivity.

[In the] On substrate 9 an ohmic contact (not shown [in Figure]) is formed by creating a thin, heavily doped semiconductor region of the same conductivity type placed between the metal (not shown[in Figure]) and [the same] substrate 9.

Over the surface of [the] semiconductor layer 10, also called an epitaxial layer, a thin silicide layer 11 is formed, for example by [a] thermal growth, made by, for example, PtNi.

[This silicide] Silicide layer 11 defines the electrical characteristics of the Schottky Barrier diode.

At the top of [the] device 8 there is, for example, a metal layer 12, deposited for all the length of [the] device 8. This metal layer 12 is made

by aluminum and it acts as an electrode 14, [called] forming the anode.

[The epitaxial] Epitaxial layer 10 makes a common drain layer for [the] device 8 and, inside said epitaxial layer 10, it [makes] also includes a plurality of regions 13, [also] called columns, of an opposite conductivity type.

[In fact the] The p type columns 13 are [opportunely] optimally doped to balance the charge on [the] n type zone 10. When this condition is reached, the electric field upon the entire volume of the drain region 10is constant and it is also equal to the critical electric field of the silicon.

This embodiment allows [to sustain] a high voltage [also in presence of a little] to be sustained while maintaining low resistivity [of the] in n type zone 10.

As a result of the presence of [the] regions or columns 13, it is possible, therefore, to reduce the resistivity of [the] epitaxial layer 10 without decreasing the breakdown voltage of the Schottky barrier diode 8, because the breakdown voltage depends on the resistivity and on the thickness of the portions of the common drain layer 10 beneath the metal layer 12.

Substantially the presence of [the] doped regions 13 under [the] metal layer 12 allows achievement of the desired breakdown voltage and capability of current transportation even with an epitaxial layer having a lower resistivity than that necessary with respect [with the] to conventional Schottky barrier diodes.

To form the doped regions 13 a p - type dopant, such as boron, is implanted.

[In fact during] During the growth of [the] epitaxial layer 10, that involves a thermal process[,] and the p type dopant diffuses vertically into [the] epitaxial layer 10 to form a plurality of bubbles 23[, so] to realize the

p type columns 13.

[In fact the innovative] The Multi Drain process of the present invention provides that the p type columns 13 are made by a sequence of successive growths of the n type epitaxial layer 10 and by [a] p type dopant implants. This is possible by means of suitable masks that localize the p type bubbles 23 in [the] n type epitaxial layer 10.

A successive thermal process modifies the p type bubble sequences into the p type columns 13.

The dopant concentration of the p type columns 13, together with their geometrical disposition and size, is suitable to sustain the desired high voltage.

The dose of these implants ranges, for example, from 1 x 10^{12} to 5 x 10^{13} at / $\text{cm}^{\square 2}$.

As a consequence of the decreased resistivity of the epitaxial layer 10, the on - resistance of the device 8 is reduced, [so to] and the current flux coming from the anode electrode and flowing towards the substrate 9 encounters a lower resistance.

However, while in conventional Schottky barrier diodes the resistivity of the epitaxial layer 10 is determined on the basis of the desired breakdown voltage, in the present invention the epitaxial layer 10 has a resistivity which is lower than the necessary to achieve the same desired breakdown voltage.

For example in a device working at 500 V, implemented with traditional technology, a resistivity of about 20 Ohm * cm is [to be] used, while with the present invention the resistivity can be less than 5 Ohm * cm.

Therefore the Multi Drain structure of the present invention allows a [to reach] higher value of breakdown voltage to be attained.

Moreover, to improve the value of the breakdown voltage it is necessary to increase the height of the p type columns 13.

Referring to Figure 2, the semiconductor layer 10 is epitaxially grown over the heavily doped substrate 9, and the thickness of the epitaxial layer 10 depends on the voltage class for which the device is provided [for].

In this specific embodiment for a Schottky barrier diode operating at about 600 V, the thickness of the metal layer 12 is about few μm, the epitaxial layer 10 can have a thickness of more than 40 μm and a value of doping of about 9×10^{14} cm^{-3} and the substrate 9 can have a value of doping of about 2×10^{19} cm^{-3}.

In Figure 3 a second embodiment of a Multi Drain Schottky barrier diode according to the present invention is shown.

As shown in [such] Figure 3, a part of the elements already described in Figure 2, a plurality of body regions 15, made by the opposite conductivity type of the drain layer, is shown.

In the specific embodiment, the drain layer or epitaxial layers 10 are made by an n - type semiconductor and therefore the plurality of columns 13 is made by a p - type semiconductor. [and the] The body regions 15 are made by heavily doped p + - type semiconductor[, that is p +].

Said p + type body regions 15, placed at the top of each p - type column 13, reduce the electric field at the surface and [by] in this way, they reduce the leakage current.

The p + type body regions 15 act as a ring guard of the force lines of the electric field and therefore they do not develop any function of contact between the drain layer and the anode electrode.

In Figure 4A a schematic cross sectional view of the Schottky

barrier diode is shown.

In [such a] Figure 4A [it is to be noted] a device 22 is shown that is [the] prior art [of] for the embodiments of the present invention illustrated successively in Figures 4 and 5.

[It is to be noted, also,] In comparing Figure 4A to Figure 1, that there is a couple 21 of p type wells on the [board] border of the metal layer 4. This metal layer 4 defines the device and limits the leakage current.

In Figure 4 and 5 a top plan view of the first embodiment of Figure 2 and a cross sectional view of the same embodiment of Figure 2 along the line V - V are shown.

Particularly in the top plan view of Figure 4 a single Schottky barrier diode with the Multi Drain structure is shown.

The Multi Drain structure comprises a plurality of p type columns 13 and a p + type ring guard 16. It is also shown an n + type channel stop 17, to prevent the leakage current.

Particularly in the cross sectional view of Figure 5 an oxide passivation layer 18, such as probimide, and the n + channel stop 17 are shown. [It] There is also shown a silicide layer 19, made, for example, of Pt, that allows [to realize] a device with a lower resistance to be realized. Moreover this silicide layer 19 is combined with a metal layer 20, made, for example, of TiNiAu, that acts as a finish of the wafer slice to improve the current flux.

It is to be noted, as shown in Figures 4 and 5, that the horizontal layout of the device, according to the present invention, is a structure that grows substantially vertically with a well defined number of p type columns, starting from a stripe layout closed around by a sequence of rings of type p. These p type rings of the board extend also vertically as a column shape.

ABSTRACT

The present invention relates to a Schottky barrier diode which contains a substrate region of a first conductivity type formed in a semiconductor material layer of same conductivity type and a metal layer. A doped region of a second conductive type is formed in the semiconductor layer, with the doped region disposed under the material layer and separated from other doped regions by portions of the semiconductor layer.